

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 6,954,083 B1  
APPLICATION NO. : 10/750232  
DATED : October 11, 2005  
INVENTOR(S) : Thornley et al.

Page 1 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 10, lines 44, 46, 50 and 52, "detector" should be changed to --detectors--.  
Lines 42-54, claim 15 should read:

--15. An integrated circuit comprising:  
a plurality of fast electromagnetic transient (EFT) fault detectors, the plurality of the EFT fault detectors being distributed across at least a portion of the integrated circuit, wherein each of the EFT fault detectors outputs a signal indicative of whether said each EFT fault detector has detected an EFT fault; and  
a logic tree that receives the signals output from the plurality of EFT fault detectors, the logic tree outputting a fault output signal, the fault output signal being indicative of whether any of the EFT fault detectors of the plurality of EFT fault detectors has detected an EFT fault.--

Column 11, lines 3, 8, and 14, "detector" should be changed to --detectors--.  
Lines 1-15, claims 18-20 should read:

--the power supply lead and the ground lead for less than two hundred nanoseconds, and wherein at least one of the EFT fault detectors detects the presence of the spike and in response thereto outputs the signal indicative of the EFT fault detector having detected the presence of an EFT fault.

19. The integrated circuit of Claim 15, wherein the integrated circuit is a standard cell integrated circuit, and wherein each of the EFT fault detectors is realized in the form of standard cell circuitry.--

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 6,954,083 B1  
APPLICATION NO. : 10/750232  
DATED : October 11, 2005  
INVENTOR(S) : Thornley et al.

Page 2 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

20. The integrated circuit of Claim 15, wherein the integrated circuit is a programmable logic device (PLD), the PLD comprising a plurality of logic blocks and a programmable interconnect structure, and wherein each of the plurality of EFT fault detectors is realized in the form of logic block circuitry.

Signed and Sealed this

Thirtieth Day of October, 2007

A handwritten signature in black ink, reading "Jon W. Dudas". The signature is stylized, with a large, looped initial "J" and a distinct "D" at the end.

JON W. DUDAS  
*Director of the United States Patent and Trademark Office*